**LTSpice Analog Entropy Override Controller - Prototype Write-Up**

**1. Circuit Description**

This LTSpice schematic (analog\_entropy\_override\_stage.asc) implements a first-stage analog logic controller designed to simulate voltage-triggered hazard response logic. It acts as a critical interface alongside a theoretical Verilog FSM, forming the analog core for Figure 3 in Paper 5. The circuit's primary function is to monitor analog "entropy" and "noise" signals, and based on these inputs, along with a digital "ML override" trigger, assert lockout or flush conditions.

The controller comprises three main sections:

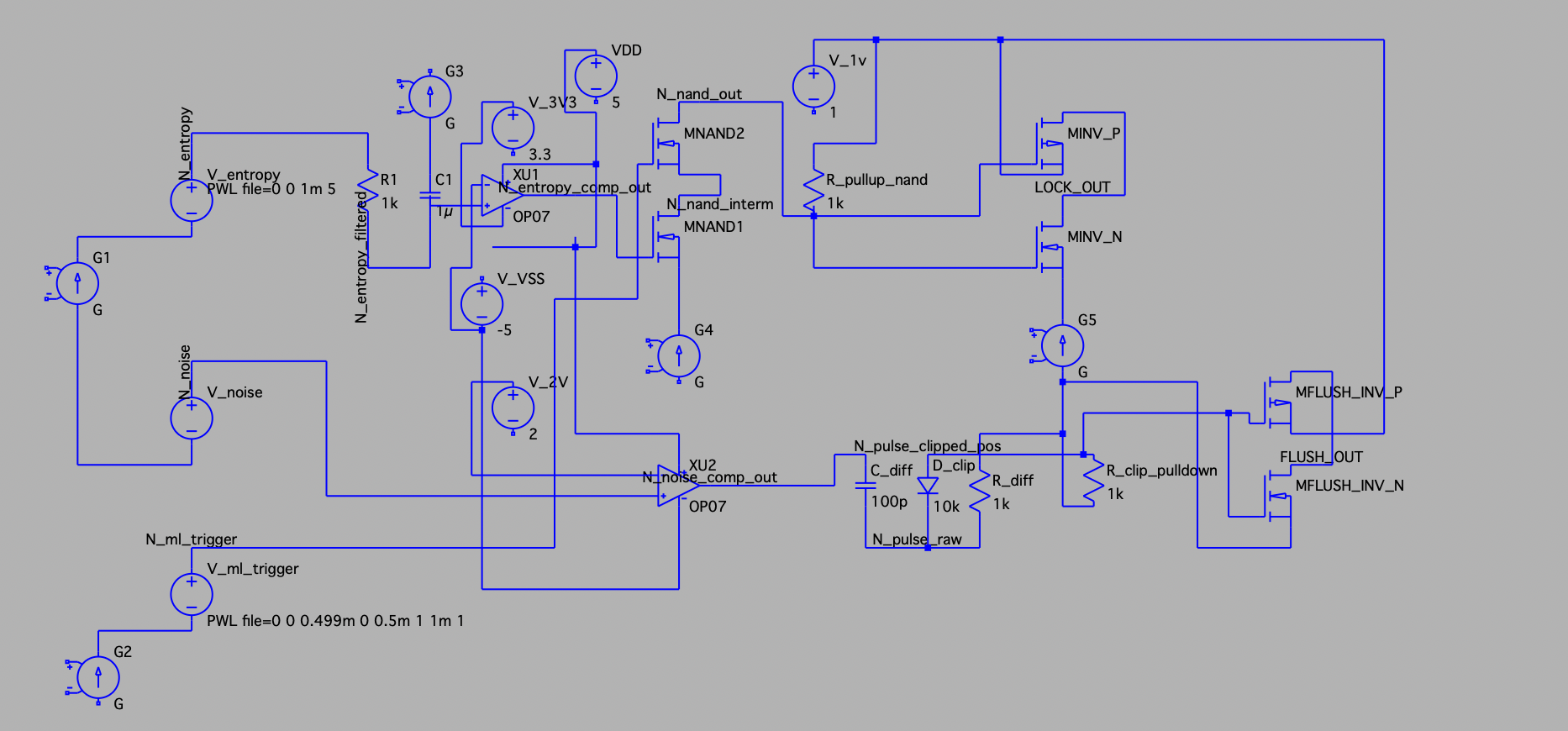
1. **Input Conditioning:** Three voltage sources simulate dynamic inputs:
   * V\_entropy: An analog voltage representing the system's entropy score.
   * V\_noise: An analog interference signal, simulating a "chaos overlay."
   * V\_ml\_trigger: A digital signal indicating when an ML-driven override is active.
2. **LOCK\_OUT Logic Block:** This section detects high entropy conditions while the ML override is active. It consists of:
   * An RC low-pass filter to smooth V\_entropy.
   * An op-amp (XU1) configured as a comparator to check if filtered V\_entropy exceeds a 3.3V threshold.
   * An NMOS-based NAND gate (formed by MNAND1, MNAND2, and R\_pullup\_nand) implementing an AND logic between the high entropy detection and V\_ml\_trigger.
   * A CMOS inverter (MINV\_N, MINV\_P) to generate the active-high LOCK\_OUT signal.
3. **FLUSH\_OUT Logic Block:** This section detects sudden spikes in the V\_noise signal to issue a brief "flush" pulse. It includes:
   * An op-amp (XU2) configured as a comparator to detect V\_noise exceeding a 2V threshold.
   * An RC differentiator (C\_diff, R\_diff) to convert the rising edge of the noise comparator's output into a short pulse.
   * A diode clipper (D\_clip, R\_clip\_pulldown) to clean up the pulse.
   * A CMOS inverter (MFLUSH\_INV\_N, MFLUSH\_INV\_P) to generate the active-high FLUSH\_OUT pulse.

Standard ideal models (N\_MOS, P\_MOS, opamp.asy, 1N4148) are used for transistors, op-amps, and the diode for simplified prototype simulation.

**2. Simulation Setup**

The circuit is configured for a time-domain (transient) simulation to observe its dynamic behavior over 1 millisecond.

* **Simulation Command:** .tran 1m
* **Input Signal Parameters:**
  + **V\_entropy (PWL):** Sweeps linearly from 0V to 5V over the 1ms simulation duration. (PWL(0 0 1m 5))
  + **V\_noise (PWL):** Generates 2.5V spikes of 50ns duration, occurring every 200ns (at 0.2ms, 0.4ms, 0.6ms, 0.8ms). (PWL(0 0 0.199m 0 0.2m 2.5 0.20005m 0 ... 1m 0))
  + **V\_ml\_trigger (PWL):** Remains at 0V until 0.5ms, then steps up to 1V and stays high for the remainder of the simulation. (PWL(0 0 0.499m 0 0.5m 1 1m 1))
* **Power Supplies:**
  + V\_VDD: +5V
  + V\_VSS: -5V
  + V\_1V\_SUPPLY: +1V (for logic outputs)
  + V\_3V3: +3.3V (reference for entropy comparator)
  + V\_2V: +2V (reference for noise comparator)
* **Component Values:**
  + R1: 1kΩ, C1: 1µF
  + R\_pullup\_nand: 1kΩ
  + C\_diff: 100pF, R\_diff: 500Ω
  + R\_clip\_pulldown: 10kΩ



**3. Simulation Results**

Upon running the transient simulation, we observed the following waveforms for the specified output nodes:

* **V\_entropy (Input):** This trace will show a smooth, linear ramp from 0V at t=0 to 5V at t=1ms. This demonstrates the simulated increasing entropy score.
* **V\_noise (Input):** This trace will display short, sharp positive spikes. You should see distinct pulses reaching approximately 2.5V at t=0.2ms, t=0.4ms, t=0.6ms, and t=0.8ms, with each pulse lasting for approximately 50ns before returning to 0V.
* **LOCK\_OUT (Output):** This signal should remain at 0V initially.
  + At t=0.5ms, V\_ml\_trigger goes high (1V).
  + V\_entropy continuously ramps up. It will cross the 3.3V threshold at approximately t=0.66ms (since it ramps from 0V to 5V over 1ms, 3.3V is 3.3/5 \* 1ms = 0.66ms).
  + Therefore, LOCK\_OUT is expected to transition from 0V to 1V at approximately **t=0.66ms** and remain at 1V until the end of the simulation. This is because both conditions (V\_entropy > 3.3V AND V\_ml\_trigger = 1V) will be met simultaneously from that point onward.
* **FLUSH\_OUT (Output):** This signal should appear as short, active-high (1V) pulses.
  + Each time V\_noise spikes above 2V (which happens at t=0.2ms, t=0.4ms, t=0.6ms, t=0.8ms), the FLUSH\_OUT signal is expected to generate a brief positive pulse.
  + These pulses will be very short, approximately 50ns in duration, mirroring the chaotic surges in V\_noise. They will quickly return to 0V between spikes.

In essence, LOCK\_OUT will be a sustained high signal triggered by a combination of high entropy and ML override, while FLUSH\_OUT will be a series of very short, reactive pulses to immediate noise events.